UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

LAF

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/152,944	09/14/98	DALLY W	81013-000-00

LMC1/0712

PILLSBURY MADISON & SURTO
INTELLECTUAL PROPERTY GROUP
1100 NEW YORK AVNEUE N W
WASHINGTON DC 20005-3918

EXAMINER	
KIM,K	
ART UNIT	**PAPER NUMBER**
2783	9

DATE MAILED: 07/12/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No. 09/152,944	Applicant(s) William J. DALLY
Examiner Ken S. Kim	Group Art Unit 2783

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 9-14-98.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-18 is/are pending in the application.

Of the above claim(s)____ is/are withdrawn from consideration.

☐ Claim(s)____ is/are allowed.

☒ Claim(s) 1-18 is/are rejected.

☐ Claim(s)____ is/are objected to.

☐ Claim(s)____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

KENNETH S. KIM
PRIMARY EXAMINER

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:____.

Attachment(s)

☒ Information Disclosure Statement(s), ~~PTO-1449, Paper~~ No(s). 6

☒ Notice of References Cited, PTO-892

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other____

Office Action Summary

1. Claims 1-18 are presented for examination.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Current title does not sufficiently reflect the inventive feature to distinguish over the prior art.

3. Applicant is requested to identify the figure best representing the invention clearly showing the novelty.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

5. Claims 3-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

(a) claim 3, it is not clear what is meant by "output vector containing values in the input data vector for which corresponding values in the condition vector are equal to a value corresponding to the output vector."

(b) Claim 7, "the limitations implied by "corresponding to condition vector values" at each occurrence are ambiguous.

(c) Claim 8, "the partial index" lacks an antecedent basis.

(d) Claim 14, "the plurality of output vectors" lacks an antecedent basis.

(e) Claim 15, it is not clear where the elements constituting the output vector come from. It is not clear whether each arithmetic cluster receives one element or all elements of the input data.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

7. Claims 1, 2, 15-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Nguyen, U.S. Patent No. 6,058,465.

Nguyen teaches the invention as claimed in claim 1 including a method of performing a conditional vector output operation in a processor comprising the steps of : (a) receiving electrical signals representative of an input data vector (col. 109; VRa), (b) generating electrical signals representative of a condition vector, the number of values in the input data vector being equal to the number of values in the condition vector, values in the input data vector and in the condition vector being in one-to-one correspondence with one another, and each value in the condition vector being a result of evaluating a predetermined conditional expression (COMPARE to VRb) using data corresponding to a value in the input data vector (col. 109),

(c) generating electrical signals representative of an output vector containing values in the input data vector for which corresponding values in the condition vector are equal to a predetermined value (col. 105), and

further teaches as in claims,

(d) wherein the predetermined conditional expression is a Boolean expression (col. 109) – claim 2, and

further teaches as in claims 15 and 16,

(e) generating a plurality of electrical signals as condition data (VMMR) representative of whether individual arithmetic clusters in a plurality of arithmetic clusters (630) are to receive data,

(f) providing a plurality of electrical signals as input data to at least one arithmetic cluster in the plurality of clusters for which a corresponding portion of the condition data is equal to a predetermined value (105, EMASK),

(g) using the arithmetic cluster to process the input data provided thereto (VCMOVM, VADD),

(h) assembling the processed data to form an output vector (Rd),

(i) wherein a certain plurality of arithmetic clusters (630) receive input data as a result of corresponding condition data for said certain plurality of arithmetic clusters being said predetermined value, and

further teaches as in claims 17 and 18,

(j) a first memory element storing an input data value (col. 105;Rb),

(k) a second memory element storing a condition value (MMASK in VMMR),

(l) a buffer element for storing an output data value (Rd),

(m) a logic circuit which transfers the input data value from the first memory element to the buffer element when the condition value stored in the second memory element is equal to a predetermined value (VCMOVM).

8. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Koyanagi et al, U.S. Patent No. 5,604,913.

Koyanagi et al teaches the invention as claimed in claim 1 including a method of performing a conditional vector output operation (figs. 1 and 2) in a processor comprising the steps of :

(a) receiving electrical signals representative of an input data vector (A; col. 1, line 50),

(b) generating electrical signals representative of a condition vector, the number of values in the input data vector being equal to the number of values in the condition vector, values in the input data vector and in the condition vector being in one-to-one correspondence with one another, and each value in the condition vector being a result of evaluating a predetermined conditional expression (MR; A>0) using data corresponding to a value in the input data vector (fig. 1; line 2),

(c) generating electrical signals representative of an output vector containing values in the input data vector for which corresponding values in the condition vector are equal to a predetermined value (MOVE instead of ADD is well known; or ADD of zero values), and

(d) wherein the predetermined conditional expression is a Boolean expression (A>0) – claim 2.

9. Claims 15 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Agarwal et al, U.S. Patent No. 5,825,677.

Agarwal et al teaches the invention as claimed in claims 15 and 16 including a method of performing a conditional vector output operation in a processor comprising the steps of :

(a) generating a plurality of electrical signals as condition data representative of whether individual arithmetic clusters in a plurality of arithmetic clusters are to receive data (col. 12, lines 11-17),

(b) providing a plurality of electrical signals as input data to at least one arithmetic cluster in the plurality of clusters (305) for which a corresponding portion of the condition data is equal to a predetermined value (col. 12, lines 11-17),

(c) using the arithmetic cluster to process the input data provided thereto (col. 12, line 16),

(d) assembling the processed data to form an output vector (col. 9, line 54),

(e) wherein a certain plurality of arithmetic clusters (305) receive input data as a result of corresponding condition data for said certain plurality of arithmetic clusters being said predetermined value.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Asai et al taught a method of sorting elements in an input vector into two output vectors according to the values in a mask vector.

Sato taught a vector processor selectively processing elements according to a mask data.

Thayer et al taught a method of conditionally moving elements in a source vector register to a destination vector register..

Inagami et al taught a method of compressing and expanding vector data elements.

11. Claims 7-13 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth S KIM whose telephone number is (703) 305-9693. The examiner can normally be reached on M-F (8:30-17:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, An T Meng-Ai can be reached on (703) 305-9678. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 306-5404 for regular communications and (703) 306-5404 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9700.

KENNETH S. KIM
PRIMARY EXAMINER